REMARKS

Claims 1-23 are pending in this application. By this Amendment, claims 1, 3-8, 10 and 11 have been amended to eliminate means-plus-function language from these claims. Thus, no new matter is added by this Amendment.

Applicants appreciate the courtesies shown to Applicants' representative by Examiner Casiano in the December 4, 2003 interview. Applicants separate record of the substance of the interview is incorporated into the following remarks.

I. Objection to the Specification

The Office Action alleges the title of the invention is not descriptive and requires a new title that is clearly indicative of the invention to which the claims are directed. To this end, Applicants have amended the title to recite "Data Transfer Control Device And Electronic Equipment For Performing Data Transfer Between A Plurality Of Nodes That Are Connected To A Bus." Applicants submit that the new title meets the requirements of the Patent Office.

Reconsideration and withdrawal of this objection are thus respectfully requested.

II. Claim Rejections Under 35 U.S.C. §102(e)

Claims 1, 10-12, 14-15, 17-18, 20-21 and 23 were rejected under 35 U.S.C. §102(e) as allegedly being anticipated by U.S. Patent No. 6,219,697 (hereinafter "Lawande"). This rejection is respectfully traversed.

Amended claim 1 recites a data transfer control device for transferring data between a plurality of nodes connected to a bus wherein the data transfer control device comprises a circuit which generates identification information for determining whether or not one received packet and the next received packet are received during different reset intervals, when a reset interval is defined as the period between a reset that clears node topology information and the next reset; and a write circuit which links each received packet with the

generated identification information, and writes the linked packet and identification information into a packet storage memory.

The present invention is directed to determining whether or not a reset occurred between the reception of one packet and the next packet, by checking for a change in the one packet and the next packet identification information. More specifically, the present invention as recited in claim 1 is directed towards a circuit which generates identification information for determining whether or not one received packet and a next received packet are received during different reset intervals, and a write circuit which links each received packet with the generated information and writes the linked packet and identification information into a packet storage memory. This procedure, and the associated benefit, of determining whether or not the packets received in different reset intervals is nowhere taught by Lawande.

Lawande is directed toward realizing IP protocol over an IEEE 1394 bus and is related to a protocol of layers higher than the protocol layers of the present invention. See IP/TCP 152, 154 and UDP 158 in Fig. 5 of Lawande. More specifically, as illustrated in Fig. 5 of Lawande, Lawande teaches a layered architecture model with the IEEE 1394 high speed serial bus 40 providing the physical and link layer functions and the IP/TCP 152, 154 serving as the transport layer. The User Datagram Protocol (UDP) is also a transport layer protocol providing connectionless mode protocol.

Fig. 6A of Lawande discloses a conventional technique related to the Bus Reset. More specifically, with reference to Fig. 6A of Lawande, Lawande teaches a bus reset state that is entered when a system power up occurs or when a node is inserted in or removed from the network. In the bus reset state, the IEEE 1394 physical layer chip detects the insertion or removal of a node and sends a reset signal onto all of the ports for a period of time to ensure

that the entire bus sees the signal. In other words, a bus reset occurs whenever the network is reconfigured by insertion or removal of a node. (See col. 12, lines 39-52 of Lawande).

Nowhere does Lawande teach or suggest a circuit which generates identification information for determining whether or not one received packet and the next received packet are received during different reset intervals, and a write circuit which links each received packet with the generated identification information and writes the linked packet and identification information into a packet storage memory, as recited in claim 1.

To further clarify, claim 1 is supported by the specification at, for example, Fig. 10 of the present application, wherein identification information (BT) is generated for determining whether or not a received packet and a subsequently received packet are received in different reset intervals. As shown by C11 of Fig. 10, each BT is linked to each packet (N to N+8) and is written to the packet storage memory. For example, packets N to N+1 and packets N+2 to N+4 are received in different bus reset intervals M and M+1. Therefore, the identification information (BT) for the packets N to N+1 and the identification information (BT) for N+2 to N+4 are different (BT is changed from 0 to 1). In this way, the processing section (firmware) can easily learn from the identification information (BT) the occurrence of a reset (bus reset) which clears node topology information (see C12, C13 and C14 of Fig. 10), thus reducing a processing load on the processing section. See page 24, line 7 to page 27, line 19 of the specification.

Further, the identification information (BT) is not changed at C15. Therefore, the identification information (BT) for received packet N+5 (BT=0) and packets N+6 to N+8 (BT=1) have different values, and the processing section learns that at least a reset has occurred between the processing of the packets N+5 and packets N+6 to N+8. In other words, although Fig. 10 illustrates the identification information as being one bit of data, the

value of BT may be two or more bits of data, such as, for example, 1, 2, 3, etc.; instead of changing from zero to one or one to zero. See page 27, lines 20-26 of the specification.

In summary, Lawande merely teaches a chip that detects insertion or removal of a node, not detecting a change in IP information between packets. Specifically, nowhere does Lawande teach or suggest determining whether a packet has been received by checking for a change in identification information between the packets, as recited in claim 1.

With respect to amended claim 10, nowhere does Lawande teach or suggest a read circuit which reads a packet from a packet storage memory when a transmission start command has been issued, as recited in claim 10.

More specifically, claim 10 recites a data transfer control device for transferring data between a plurality of nodes connected to a bus, wherein the data transfer control device comprises a read circuit which reads a packet from a packet storage memory when a transmission start command has been issued, a link circuit which provides services for transmitting read packet to each node, and a status storage register which stores status information indicating that the transmission of a packet has been halted, when the transmission of the packet has been halted by the occurrence of a reset that clears node topology information.

In other words, as supported by the specification at, for example, Figs. 17A-17D, if a reset occurs slightly before the transmission start command has been issued, the processing section cannot determine which of the cases has occurred and thus the processing stalls (see Figs. 17B and 17C). However, the status storage register stores status information indicating that the transmission of a packet has been halted due to the occurrence of a reset (see Fig. 17D). Therefore, the present invention, as defined by claim 10, allows the processing means to easily distinguish the cases (see step S41 of Fig. 18), thus preventing the processing of the

processing section from being stalled. See page 34, line 2 to page 35, line 27 of the specification).

Lawande merely teaches an interrupt to indicate the entry into Bus Reset. See col. 12, lines 53-54 of Lawande. Existing TCP connections between nodes, other than the node being inserted/removed, are not reset upon entering the Bus Reset state. See col. 12, lines 61-63.

Nowhere does Lawande teach or suggest a read circuit which reads a packet from a packet storage memory when a transmission start command has been issued, as recited in claim 10. Nowhere does Lawande teach or suggest the status storage register which stores status information indicating that the transmission of a packet has been halted, when the transmission of the packet has been halted by the occurrence of a reset that clears node topology information, as recited in claim 10. This benefit allows prevention of stalls, for example, in the processing of the hardware, even if a reset occurs slightly before the issue of a transmission start command. This benefit is nowhere taught or suggested by Lawande.

For the foregoing reasons, Applicants respectfully submit that Lawande fails to anticipate the subject matter of independent claims 1 and 10 or any of depending claims 11, 12, 14, 15, 17, 18, 20, 21 and 23. Reconsideration and withdrawal of this rejection are respectfully requested.

III. Rejections Under 35 U.S.C. §103(a)

A. Lawande

Claim 3 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Lawande. Specifically, the Office Action alleges that randomly accessible memory is well known in the art and that one of ordinary skill in the art would have been motivated to specify the cited storage means as randomly accessible in order to obtain a memory which has the information permanently placed into it. This rejection is respectfully traversed.

Claim 3 depends from claim 1 and adds that the packet storage memory is a randomly accessible storage memory and is divided into a control information area in which is stored packet control information and a data area in which is stored packet data, and that the identification information is included within the control information written to the control information area.

Even if one of ordinary skill in the art could have found Lawande to teach a packet storage memory that is a randomly accessible storage memory and is divided into a control information area in which is stored packet control information; and to teach a data area in which is stored packet data, and that the identification information is included within the control information written to the control information area, the presently claimed invention still would not have been achieved. Specifically, nothing in Lawande teaches or suggests determining whether a packet has been received by checking for a change in identification information between the packets, as discussed above with respect to claim 1.

Accordingly, Applicants respectfully submit that Lawande would not have led one of ordinary skill in the art to the invention of claim 1 or depending claim 3. Reconsideration and withdrawal of this rejection are respectfully requested.

B. Lawande in view of Robins

Claim 2 was rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Lawande in view of U.S. Patent No. 5,590,124 (hereinafter "Robins"). This rejection is respectfully traversed.

Claim 2 depends from claim 1 and adds that the identification information is a toggle bit that toggles from zero to one or from one to zero when one received packet and the next received packet are packets received within different reset intervals.

Robins was cited as allegedly teaching a toggle bit to indicate the status of a pin. The Office Action alleges that a toggle is usually associated with software configurations and it

would have been obvious to one of ordinary skill in the art to modify the disclosure by Lawande by including a toggle bit in order to incorporate an indicator for the software application.

Even if one of ordinary skill in the art could have found Robins to teach a toggle bit to indicate the status of a pin, the presently claimed invention still would not have been achieved. Specifically, nothing in Robins remedies the deficiencies of Lawande discussed above with respect to claim 1. That is, nothing in the combined teachings of Robins and Lawande would have led one of ordinary skill in the art to a data transfer control device comprising means which generates identification information for one received packet and the next received packet, wherein whether or not the one received packet and the next received packet are received during different reset intervals is determined by checking for a change in the identification information between the one received packet and the next received packet, wherein a reset interval is defined as the period between a reset that clears node topology information and the next reset, as recited in claim 1.

Accordingly, Applicants respectfully submit that Robins and Lawande, whether taken singularly or in combination, would not have led one of ordinary skill in the art to the invention of claim 1 or depending claim 2. Reconsideration and withdrawal of this rejection are thus respectfully requested.

C. Lawande in view of Gehman

Claims 4-9, 13, 16, 19 and 22 were rejected under 35 U.S.C. §103(a) as allegedly being unpatentable over Lawande in view of U.S. Patent No. 6,304,553 (hereinafter "Gehman"). This rejection is respectfully traversed.

As acknowledged by the Patent Office, Lawande does not teach a first pointer storage means for storing pointer information that specifies a boundary in the package storage means.

However, the Patent Office alleges that Gehman teaches a data transfer control device where pointer information specifies a boundary in storage.

The Patent Office referenced col. 5, lines 48-59 of Gehman where it is stated "the removal is accomplished by storing or remembering the FIFO right pointer location before writing the 1394 header."

Claim 4 recites a first pointer storage register which stores first pointer information that specifies a boundary in the packet storage memory between an area for a packet received before the occurrence of a reset that clears node topology information and an area for a packet received after the occurrence of the reset. The configuration recited in claim 4 allows avoidance of hardware processing stalls by enabling preferential processing of a packet received after the reset has occurred.

Specifically, as shown in Fig. 12 of the present application, the first pointer information storage register BPR stores first pointer information BP that specifies a boundary RBI in the packet storage memory between an area of a packet received before the occurrence of a reset that clears node topology information and an area for a packet received after the occurrence of the reset. In this way, the processing section (firmware) may easily distinguish a packet received before the occurrence of a reset from a packet received after the occurrence of the reset, and thus reducing a processing load on the processing section (see Fig. 13B and 13C). See page 28, line 1 to page 34, line 1. This benefit is nowhere taught by Lawande or Gehman, alone or in combination.

Nowhere do Lawande and Gehman teach or suggest a first pointer storage register which stores first pointer information that specifies a boundary in the packet storage memory for an area for a packet received before the occurrence of the reset that clears node topology information and an area for a packet received after the occurrence of the reset, as recited in claim 4.

Further, Lawande and Gehman, alone or in combination, fail to disclose a second pointer storage register which stores second pointer information that specifies a boundary in the packet storage memory between an area for processed packets and an area for unprocessed packets, and a third pointer storage register which stores third pointer information which specifies a boundary in the packet storage memory between an area for received packets and an area storing no received packets, as recited in claim 6.

Still further, Lawande and Gehman, alone or in combination, fail to disclose a fourth pointer storage register which stores fourth pointer information which specifies a boundary in the control information area between control information for a packet received before the occurrence of the reset that clears node topology information and control information for a packet received after the occurrence of the reset, and a fifth pointer storage register which stores fifth pointer information which specifies a boundary in the data area between data of a packet received before the occurrence of the reset that clears node topology information and data of a packet received after the occurrence of the reset, as recited in claim 8.

Accordingly, Applicants respectfully submit that Lawande and Gehman, alone or in combination, do not teach or suggest the features of independent claim 4, depending claims 6 and 8 or any of depending claims 5, 7, 9, 13, 16, 19 and 22. Reconsideration and withdraw of this rejection are thus respectfully requested.

IV. Conclusion

In view of the foregoing, it is respectfully submitted that this application is in condition for allowance. Favorable reconsideration and prompt allowance of claims 1-23 are earnestly solicited.

Should the Examiner believe that anything further would be desirable in order to place this application in even better condition for allowance, the Examiner is invited to contact the undersigned at the telephone number set forth below.

Respectfully submitted,

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